REMARKS

Summary of Office Action

Claims 1-32 are pending in this application.

Claims 1-7 and 26 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Sugiyama U.S. Patent No. 6,396,872 ("Sugiyama"). Claims 12-17, 28 and 29 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Debus, Jr. U.S. Patent No. 4,773,034 ("Debus"). Claims 22, 23 and 31 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Tomisato et al. U.S. Patent No. 5,504,783 ("Tomisato").

Claims 8-11, 24, 25, 27 and 32 have been rejected under 35 U.S.C. § 103(a) as being obvious from Lu U.S. Patent No. 6,275,836 ("Lu") in view of Shanbhag et al. U.S. Patent No. 6,940,898 ("Shanbhag") further in view of Debus. Claims 18-21 and 30 have been rejected under 35 U.S.C. § 103(a) as being obvious from Hillery U.S. Patent No. 6,178,201 ("Hillery") in view of Wang et al. U.S. Patent No. 6,693,958 ("Wang").

Summary of Applicants' Reply

Applicants have amended claims 1, 8, 12, 17, 18, 22, 24, and 26-32 in order to more particularly define the claimed invention. No new matter has been added and the amendments are fully supported by the originally-filed specification. (See, e.g., applicants' specification at p. 7, ¶ 18, p. 9, ¶ 23, and p. 10, ¶ 27.)

Applicants respectfully traverse the Examiner's rejections.

Reply to the Prior Art Rejections

Claims 1-7 and 26

Claims 1-7 and 26 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Sugiyama. This rejection is respectfully traversed.

Applicants' invention, as defined by amended independent claims 1 and 26, is directed to circuitry and a method for adaptively equalizing a received data signal. An equalization implementation circuitry that includes a selectable number of taps operates on the received data signal. Selection circuitry is programmed to select between a first and a second number as the selectable number of taps only once while the equalization implementation circuitry operates on the received data signal.

Sugiyama generally describes adaptive filters 60 that are operated by initial number of taps stored in memory circuit 25, the approximate number of taps calculated in the calculation circuit of approximate numbers of taps 20 and subsequently by the optimum number of taps caculated in the tap assignment control circuit 10. A selection circuit 26 performs the selection of the taps source in accordance with a timing signal supplied from control circuit 27. (Sugiyama, FIG. 1, Abstract and col. 11, lines 32-60.)

Applicants respectfully submit that Sugiyama does not show or suggest selection circuitry programmed to select

between a first and a second number as the selectable number of taps only once while the equalization implementation circuitry operates on the received data signal, as defined by claims 1 and 26. In the Sugiyama device, selection circuit 26 performs the selection of the taps provided to adaptive filters 60 in accordance with a timing signal supplied from control circuit 27 and thus the selected tap changes as the adaptive filters operate on the data signal. Nowhere does Sugiyama show or suggest that the selection circuitry is programmed to select between two taps only once while the equalization implementation circuitry operates on the received data signal. Thus, Sugiyama does not show or suggest show all the features of applicants' claims 1 and 26.

Moreover, nowhere does Sugiyama show or suggest that the any of the elements used in the adaptive filters are implemented on a programmable logic device, as required by the claims. Thus, Sugiyama cannot show or suggest that the selection circuitry is programmed to perform a selection.

Accordingly, applicants respectfully submit that independent claims 1 and 26 and claims 2-7 that depend, directly or indirectly from claim 1, are allowable.

Claims 8-11, 24, 25, 27 and 32

Claims 8-11, 24, 25, 27 and 32 have been rejected under 35 U.S.C. § 103(a) as being obvious from Lu in view of Shanbhag further in view of Debus. This rejection is respectfully traversed.

Applicants' invention, as defined by amended claims 8, 24, 27 and 32, is directed to circuitry and a methods

for adaptively equalizing a received data signal. An equalization implementation circuitry that includes taps having a selected one of either integer spacing or fractional spacing relative to the symbol rate of the data signal operates on the received data signal (claims 8 and 27) or includes at least one sampling point with a selectable location (claims 24 and 32). Selection circuitry is controlled by a programmable element to select only once between first and second selections for integer spacing or fractional spacing (claims 8 and 27) or to select only once between a first and second location as the selectable location (claims 24 and 32) while the equalization implementation circuitry operates on the received data signal.

Lu generally describes an interpolation filter used in a transmission system for producing either fractional or integer interpolation ratios. A controller 74 determines whether the integer or fractional interpolation ration is needed based on a sampling data rate received from the filter. (Lu, FIG. 3, Abstract and col. 7, lines 16-28.)

Debus generally describes an adaptive equalizer that includes a rotating coefficient register 212 that successively associates each coefficient with a multiply-accumulate device. Circuit 214 provides for the insertion of a specific coefficient value and circuit 215 automatically adjusts the coefficients to their optimal values. The selection of whether circuit 214 or 215 is used to provide the coefficient values is determined by manually toggling switch 230. (Debus, FIG. 2, Abstract, col. 3, lines 8-25.)

The Examiner acknowledges that Lu does not teach selection of one of the first and second selections as the selected one of integer spacing and fractional spacing and cites Debus as allegedly making up for this deficiency (Office Action, page 7, paragraph 3).

Applicants respectfully submit that neither Lu nor Debus, whether taken alone or in combination, show or suggest selection circuitry controlled by a programmable element to select only once between first and second selections for integer spacing or fractional spacing or to select only once between a first and second location as the selectable location while the equalization implementation circuitry operates on the received data signal, as defined by claims 8, 24, 27 and 32. First, Debus discusses a switch 230 that is manually toggled to select between manual coefficient value 214 and auto coefficient update 215 and does not show or suggest selection circuitry that is controlled by a programmable element. Moreover, neither Lu nor Debus shows or suggests the adaptive equalizer being implemented on a programmable logic device and thus neither can show or suggest control of a selection circuit by a programmable element. Second, even if controller 74 in the Lu device were a programmable element, which it is not, controller 74 selects a desired switch 76 based on the incoming data sampling rate and is not programmed to select only once while equalization circuitry operates on the received data signal (Lu, col. 7, lines 20-24). Thus, even if Lu were to be combined with Debus, the combination fails to show all the features of applicants' claimed invention because neither Lu

nor Debus shows or suggests a switch controlled by a programmable element to select only once while equalization circuitry operates on the received data signal.

Applicants remind the Examiner "[t]hat mere fact that a worker in the art could rearrange the parts of the reference device to meet the terms of the claims ... is not by itself sufficient to support a finding of obviousness. The prior art must provide a ... reason for the worker in the art, without the benefit of appellant's specification, to make the necessary changes in the reference device." Ex parte Chicago Rawhide Mfg. Co., 223 USPQ 351, 353; MPEP § 2144.04. The Examiner's position requires one to rearrange and modify the Lu system in the following two ways: a) manual coefficient update 214 and switch 230 of Debus would have to be added to the Lu device and b) switch 230 would have to be modified to be programmable to perform a one-time selection between controller 74 and manual coefficient update 214. Neither of these two necessary modifications is supported by either the Lu or the Debus disclosure (or any other reference for that matter). Thus, there is no reason for the worker in the art to make such changes without the benefit of applicants' specification. Therefore, the Examiner's position with regard to applicants' selection circuitry is insufficient as a matter of law to support a finding of obviousness. Moreover, Debus discusses circuits 214 and 215 being used to provide coefficient values to the multiply-accumulate device of an adaptive equalizer and not to provide selections for integer spacing or fractional spacing or a selectable location for a sampling point. Thus,

one skilled in the art would not find the teachings of Debus useful in modifying Lu in the manner suggested by the Examiner to show applicants' claimed invention.

Shanbhag is cited by the Examiner as allegedly showing other features of the claims and does not make up for the deficiencies of Lu or Debus relative to the rejection.

Accordingly, applicants respectfully submit that independent claims 8, 24, 27 and 32 and claims 9-11 and 25 that depend, directly or indirectly from claim 8 or 24, are allowable.

Claims 12-17, 28 and 29

Claims 12-17, 28 and 29 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Debus. This rejection is respectfully traversed.

Applicants' invention, as defined by amended claims 12, 17, 28 and 29, is directed to circuitry and a methods for adaptively equalizing a received data signal. An equalization implementation circuitry includes a selectable coefficient value. A first processing circuitry computes the coefficient value using a selectable starting value, where the coefficient value is different from the starting value. Selection circuitry selects one of a first and a second starting value as the selectable starting value, where the selection circuitry is controlled by a programmable element.

Debus generally describes an adaptive equalizer that includes a rotating coefficient register 212 that successively associates each coefficient with a multiply-accumulate device. Coefficient register 212 is formed by delay elements 211, 221

and 231 serially interconnected in a continuous loop. The selection of whether circuit 214 or 215 is used to provide the coefficient values is determined by manually toggling switch 230. (Debus, FIG. 2, Abstract, col. 3, lines 8-25.)

The Examiner alleges that Debus shows all the features of applicants' claimed invention in showing that registers 212 compute coefficient values using a starting value provided by manual coefficient update 214 or auto coefficient update 215. Applicants respectfully disagree.

Applicants respectfully submit that Debus does not show or suggest processing circuitry that computes the coefficient value using a selectable starting value, where the coefficient value is different from the selectable starting value, as defined by claims 12, 17, 28 and 29. Instead, in Debus registers 212 receive a coefficient value (or selectable starting value) from circuits 214 or 215 and add a delay to the received value using delay elements 211, 221 and 231. Because in Debus the coefficient that is received and delayed nevertheless maintains the same value, Debus does not show or suggest that the coefficient value is different from the selectable starting value. Thus, Debus does not show or suggest all the features of applicants' claims 12, 17, 28 and 29.

Moreover, as discussed above, because in Debus switch 230 is manually toggled it is not controlled by a programmable element, as required by applicants' claims 12, 17, 28 and 29. Thus, Debus does not show or suggest this features of applicants' claims.

Accordingly, applicants respectfully submit that claims 12, 17, 28 and 29 and claims 11-16 that depend, directly or indirectly from claim 12, are allowable.

Claims 18-21 and 30

Claims 18-21 and 30 have been rejected under 35 U.S.C. § 103(a) as being obvious from Hillery in view of Wang. This rejection is respectfully traversed.

Applicants' invention, as defined by amended claims 18 and 30, is directed to circuitry and a method for adaptively equalizing a received data signal. An equalization implementation circuitry responsive to an error signal operates on the received data signal. Selection circuitry is programmed to select between a first and a second error signal as the error signal only once while the equalization implementation circuitry operates on the received data signal.

Hillery generally describes an adaptive equalizer that includes a multiplexer 36 that selects between a first error generator 38 and a second error generator 40. The selection is controlled by error signal selector 34 which includes a state machine and a set of condition generators and switches between the error signals in response to a set of control signals reflecting the status of a convergence operation. (Hillery, FIG. 1, Abstract and col. 4, lines 33-41.)

Applicants respectfully submit that Hillery does not show or suggest selection circuitry programmed to select between a first and a second error signal as the error signal for the equalization implementation circuitry only once while

the equalization implementation circuitry operates on the received data signal, as defined by claims 18 and 30. In the Hillery device, error signal selector 34 performs the selection of the error signal in response to control signals which reflect status of convergence and thus the selected error signal changes as the adaptive equalizer operates on the data signal. Nowhere does Hillery show or suggest that the selection circuitry is programmed to select between two error signals only once while the equalization implementation circuitry operates on the received data signal. Thus, Hillery does not show or suggest show all the features of applicant's claims 18 and 30.

Moreover, nowhere does Hillery show or suggest that the any of the elements used in the adaptive equalizer are implemented on a programmable logic device, as required by the claims. Thus, Hillery cannot show or suggest that the selection circuitry is programmed to perform a selection.

Wang is cited by the Examiner as allegedly showing other features of the claims and does not make up for the deficiencies of Hillery relative to the rejection.

Accordingly, applicants respectfully submit that claims 18 and 30 and claims 19-21 that depend, directly or indirectly from claim 18, are allowable.

Claims 22, 23 and 31

Claims 22, 23 and 31 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Tomisato. This rejection is respectfully traversed.

Applicants' invention, as defined by amended claims 22 and 31, is directed to circuitry and a method for adaptively equalizing a received data signal. Processing circuitry computes an error signal using a selectable training pattern, where the processing circuitry operates on the received data signal. Programmable circuitry allows a first training pattern to be specified and training pattern circuitry provides a second training pattern. Selection circuitry selects one of the first and second training patterns as the selectable training pattern only once while the processing circuitry operates on the received data signal.

Tomisato generally describes a frequency diversity transmitter and receiver. Channel impulse response estimation is carried out using the training signal of one hopping channel (e.g., group #3). However, if the proportion of group #4 exceeds the proportion of group #3 which hits, then it is the training signal of group #4 that is used. The hopping channel giving the smaller error is judged to be the one with the greater hitting proportion. (Tomisato, Abstract, col. 19, line 25 to col. 20, line 20.)

Applicants respectfully submit that Tomisato does not show or suggest training pattern circuitry that provides a training pattern and selection circuitry that selects between two training patterns as the selectable training pattern only once while a processing circuitry operates on a received data signal, as defined by claims 22 and 31. First, nowhere does Tomisato discuss a training pattern circuitry that provides a training pattern. Tomisato discusses the training signals as

being received over a transmission channel and thus does not show or suggest the training pattern being provided by training pattern circuitry. Second, even if Tomisato did show training patter circuitry that provides a training pattern, which it does not, in Tomisato the training pattern is selected based on the signal that has the greatest hitting proportion and thus is not selected only once while a processing circuitry operates on a received data signal. Therefore, Tomisato does not show or suggest show all the features of applicant's claims 22 and 31.

Accordingly, applicants respectfully submit that claims 22 and 31 and claim 23 that depends from claim 22, are allowable.

Conclusion

The foregoing demonstrates that claims 1-32 are allowable. This application is therefore in condition for allowance. Reconsideration and prompt allowance are accordingly respectfully requested.

Respectfully submitted,

/Gall C. Gotfried/

Gall C. Gotfried
Registration No. 58,333
Agent for Applicants
FISH & NEAVE IP GROUP
ROPES & GRAY LLP
Customer No. 36981
1211 Avenue of the Americas
New York, New York 10036-8704
Tel: (212) 596-9000